ABSTRACT

Methods of reducing a short channel phenomena for an NMOS device formed in an SOI layer, wherein the short channel phenomena is created by boron movement from a channel region to adjacent insulator regions, has been developed. A first embodiment of this invention entails the formation of a boron or nitrogen doped insulator layer located underlying the NMOS device. This is accomplished via formation of shallow trench openings in composite silicon nitride - silicon shapes, followed by lateral pull back of the silicon nitride shapes exposing portions of the top surface of the silicon shapes, followed by implantation of boron or nitrogen ions into portions of the insulator layer exposed in the STI openings and into portions of the insulator layer underlying exposed portions of the silicon shapes. A subsequent hydrogen anneal procedure finalizes the doped insulator layer which alleviates boron segregation from an overlying NMOS channel region. A second embodiment features the formation of a dielectric barrier layer on the surfaces of STI openings preventing boron from segregated to silicon oxide filled STI regions. A combination of both embodiments can be employed to reduce and prevent boron segregation to both underlying and adjacent insulator regions, thus reducing the risk of short channel phenomena.